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High-T_c edge-gcomdry SNS weak links on silicon-on-sapphire substrates

13. D. Hunt, M. C. Foote, W. T. Pike, .1. 11. Barner, and R. P. Vasquez

Center for Space M croelectronics Technology, Jet l'repulsion 1 aboratory,

California nstitute of Technology, Pasadena, CA 91109

Abstract

1 ligh-quality superconductor/normal-metal/superconductor (SNS) edge-geometry weak links have been produced on silicon-on-sapphire (S0S) substrates using a new $SrTiO_3$/"seed-layer"/cubic-zirconia (YSZ) buffer system. The seed layer is a thin $YBa_2Cu_3O_{7-x}$ (YBCO) or $PrBa_2Cu_3O_{7-x}$ (PBCO) film, which provides a template for growth of the $SrTiO_3$. This multilayer buffer system eliminates problems with series grain boundary weak links seen in edge junctions on single YSZ buffer layers on SOS, while the use of moderate-dielectric-constant SOS substrates should benefit high-frequency applications and enable integration with silicon circuitry. SNS weak links fabricated on SOS with PBCO and Co-doped-YBCO normal metal layers exhibit current-voltage characteristics qualitatively consistent with the resistively-shunted-junction mode], with modulating ac-Josephson steps and operation to temperatures above 77 K. These arc the first reported epitaxial edge-geometry SNS devices on SOS substrates.

Keywords: applications of high-T_c superconductors, Josephson effect, multilayers, weak links, SNS, silicon-on-sapphire, $YBa_2Cu_3O_{7-x}$

Running Title: 1 ligh-T_c SNS weak links on SOS substrates

1. Introduction

Excellent progress has been made over the past few years in the development of high-temperature superconductor (11'1'S) Josephson weak links utilizing a variety of different device technologies. One of the most promising approaches is an epitaxial edge-geometry SNS device structure using an oxide normal metal deposited on an ion-milled YBCO base electrode edge [1 ,2,3,4,5,6]. While the devices still require further optimization, these HTS weak links are approaching the quality needed for a number of high frequency applications including Josephson mixers for sub-mm wave receivers, local oscillators for mixers, and ultra-high speed logic circuits. Such high frequency applications often require low-to-medium dielectric constant substrates ($\varepsilon \lesssim 12$) in order to optimize coupling to the active elements (e.g. waveguide mixers) and to maximize the propagation velocity in circuit interconnects. An additional influence on substrate choice is the fact that many applications would also benefit from the ability to integrate silicon and superconductor circuitry on the same substrate. However, acceptable substrates for 11'1'S film growth are limited by the requirements for a reasonable lattice match to the oxide superconductor, as well as chemical compatibility with the superconductor at the growth temperature. 111 part because of these constraints, most HTS film growth and device studies have been done on much higher-ciiclcclric-constant substrates, such as $LaAlO_3$ ($\varepsilon \approx .25$) or $SrTiO_3$ ($\varepsilon \approx 300$).

Recent progress in buffer layer technology has relaxed some of the limitations 011 substrate selection, and made new substrate choices possible. A number of groups have demonstrated that high quality epitaxial YBCO films can be grown on YSZ and other buffer layers on Si [7,8,9,1 **0,11,** 12] and Si-on-sapphire (S0S) substrates [13, 14]. These substrates are attractive for high frequency applications because they have moderate dielectric constants ($\varepsilon_{Si} \approx 12$, $\varepsilon_{SOS} \approx 9$-11) and allow for the possibility of Si device integration. However, Y BCO films grown on Si suffer fi om cracking and aging problems in layers thicker than about 500 Å due to strain induced by differential thermal contraction during cooling from the growth temperature [S, 1 i]: The a-b average of the YBCO mean thermal expansion coefficient, α_m, from 20-S00"[" is 15 x 10^{-6}/ °C [15], while for Si, α_m (20-800°C) = 3.8 x 10^{-6} / °C [1 6]. Silicon-on-sapphire is a better substrate for 11'1'S high-

frequency device fabrication for a variety of reasons. Sapphire has a thermal expansion coefficient more closely matched to YBCO (for sapphire, α_m(20 -800" C) = 8.2 x 10^{-6} / °C, averaged over the a and c-axis directions [1 6]), and YBCO films as thick as 4000 Å can be grown on SOS substrates without cracking [13]. S0S substrates are also robust and have low high-frequency losses. in addition, silicon-on-sapphire growth technology has developed to the point that SOS wafers with CMOS-quality Si are commercially available. An important point is that the Si epilayer does not hinder the growth of high-quality YBCO overlayers. in fact, with the proper buffer layer technologies, better quality YBCO films have been grown on silicon-on-sapphire than on buffer layers directly on sapphire substrates [13, 14].

Most research to date has focused on optimization of single-layer YBCO film growth on various buffer layers on SOS substrates, but Burns, et al. have recently reported the fabrication of WI'S grain-boundary junctions and flux-flow transistors combined with small-scale CMOS circuits on the same SOS chip [17]. However, to out knowledge, there have been no reports of epitaxial SNS edge-geometry weak links on any ll~odcratc-dielectric-corjst:lr~t substrates, including Si and SOS. This may be partly due to the fact that the fabrication of edge-geometry weak links is complicated by additional restrictions on the choice of substrate and associated buffer layers, since good epitaxy must be maintained across the interface between the YBCO base electrode and the underlying material. Such a requirement is nontrivial, because some commonly-used buffer layers form interracial reaction layers with YBCO and arc not lattice-matched to YBCO in the c-axis. These points arc discussed in more detail below.

This paper reports on YBCO film growth and the fabrication of epitaxial edge-~co]nctry SNS weak links on several different buffer layer combinations on SOS substrates. In brief, it is found that, while high-quality single-laycl YBCO films can be grown on YSZ buffer layers, edge-geometry weak links fabricated On YSZ exhibit problems with series grain-boundary weak links. However, high quality SNS edge junctions can be produced on $SrTiO_3$. In order to obtain high quality epitaxial $SrTiO_3$ layers on SOS, wc have developed a Sr'l"iO~/''sccla yereYSZ/YSZ buffer system in which a YBCO or I'llCC) seed layer provides a template for growth of the $SrTiO_3$ top layer. Without the seed

layer, the $SrTiO_3$ does not grow epitaxially, and YBCO overlayers are not superconducting. The present study differs from previous HTS device work on SOS substrates in its focus on epitaxial SNS devices, as well as the fact that the HTS weak links are produced directly over buffer layers on the underlying Si epilayer, rather than on a portion of the substrate where the Si has been etched away [1 7]. This approach allows, in principal, three-(iinwnsional integration of Si and HTS circuits, as well as superconducting interconnect runs above underlying Si circuitry, although nonepitaxial por tions of the Si circuit (e.g. the MOS gates) would have to be avoided.

2. Edge-geometry SNS weak link fabrication

The basic device structure used in this work is an c(i~c-geometry SNS weak link, as shown in Figure 1 (a). The device consists of a c-axis-oriented YBCO base electrode with an exposed edge. An epitaxial normal metal is deposited on the YBCO edge, followed by deposition of the YBCO counterelectrode. Because the top surface of the base electrode is covered by a thick insulator, electrical contact between the YBCO electrodes is confined to the edge of the lower YBCO film. This geometry has the advantages that the critical N/S interfaces are located on the longer-coherencc. length YBCO Surfaces, and that submicron device areas can be realized using conventiona photolithography. In addition, the effective microbridge length is determined by the normal recta thickness, and therefore very short, precisely-controlled bridge lengths (and hence critical currents) arc achievable. The edge geometry also simplifies basic circuit fabrication because tbc counterelectrode serves as the wiring layer, and no additional epitaxial insulator and superconductor layers arc needed, in contrast to sandwich-geometry, trilayer junctions.

Details of the film deposition and edge-geometry weak-link fabrication processes have been described previously [2,5,1 8,19,20], but will be briefly summarized here, including some recent process changes made to improve YBCO film quality and device yield. Device fabrication begins with pulsed laser deposition (PI .D) of a c-axis-oriented YB CO thin film onto a substrate or previously deposited buffer layers. The 1'1.1> process is generally done at a target-to-substrate distance of 5 cm at an oxygen pressure of approximately 400 mT. The laser beam is scanned radially

over a rotating 2 inch diameter target, and the substrate is oscillated approximately one cm from side to side, parallel to the target surface to achieve better film uniformity. Our recent device work has utilized ablation targets of nominal composition $YBa_{1.95}La_{0.05}Cu_3O_{7-x}$, because a small amount of La doping is reported to produce higher YBCO transition temperatures [21]. We have found that the combination of working at relatively short target-to-substrate distances and using the La-doped YBCO target has resulted in better YBCO film quality and reproducibility with typical transition temperatures ranging from 89 to 91.5 K. Following growth of the base electrode, a thin (1 00-300 Å), nonepitaxial MgO, YSZ, or $SrTiO_3$ passivation layer is deposited over the YBCO before removal from the laser ablation chamber. Work is also in progress to develop all-epitaxial YBCO-insulator bilayers to allow superconducting wiring runs above the base electrode. Next a thick (≈ 0.3 to 0.8μm) MgO, YSZ, or $SrTiO_3$ layer is deposited by e-beam evaporation or PI .D and patterned using a chlorobenzene or reversal-process photoresist liftoff stencil. The best liftoff results have been obtained using an AZ 5214 photoresist reversal process with AZ developer mixed 1:1 with water. The patterned insulator film is utilized as an ion milling mask with 300-500 CV Ar ions at a milling angle of 60° from the substrate normal to produce a tapered edge in the YBCO base electrode. For early samples the edge cutting step was sometimes followed by a low energy (50eV) ion cleaning step, but we have found more recently that this cleaning, is not essential for fabrication of high quality devices with this all-in-situ process. Just after milling of the YBCO edge, within the same vacuum system, the normal metal layer and YBCO counterelectrode are deposited at growth temperatures of ≈ 775-800 C. A lithography and ion milling step is then used to pattern via holes down to the base YBCO film and to liftoff Au contact pads. Finally, another lithography and milling step defines the counterelectrode. Completed devices have nominal counterelectrode widths ranging from 25 μm to 1.25 pm.

A key requirement in fabrication of edge-geometry SNS weak links is prevention of the formation of a grain boundary in the YBCO counterelectrode below the device edge (see Figure 1 (b)). Such a grain boundary is undesirable because it forms an additional weak link in series with the SNS weak link at the base electrode edge. Nucleation of a counterelectrode grain boundary can

be prevented, in part, by tapering the base electrode edge using an angled ion milling process, as described above [18, **19,22].** However, it is also important to note that, because ion milling is a nonselective etching process, the edge-cutting step inevitably mills at least partially into the substrate or buffer layers below the YBCO base electrode edge. As a result, the normal metal and counterelectrode must grow over the base-electrode/substrate (or buffer layer) interface. If the c-axis lattice constant of the substrate or buffer layer does not match that of YBCO, or a YIICO-substrate (buffer layer) reaction layer exists, epitaxial growth of the normal metal and counterelectrode may be disrupted, resulting in formation of a grain boundary in these layers, as shown in Figure 1(b). q'bus, for fabrication of reproducible, high-quality edge-geometry weak links, it is important to usc substrates or buffer layers which provide a c-axis lattice match, and do not form a reaction layer at the YBCO interface. As will be seen in the next section, these arguments arc consistent with problems seen in device fabrication on YSZ buffer layers on silicon-on-sapphire.

A number of other buffer layers that enable high-quality single layer YBCO film growth on Si or SOS have been reported. However, these buffer layers may also be unsuitable for edge-geometry weak link fabrication for the reasons presented above. For example, a YSZ/CeO_2 buffer layer system has been shown to produce excellent quality YBCO films on SOS [14], but CeO_2 may not be ideal for edge junction fabrication because it dots not lattice match YBCO in the c-axis (CeO_2 is cubic with a = 5.41 Å), and a YBCO-CeO_2 reaction layer is known to form for growth temperatures near 790 °C [23]. Similarly, although high-quality YBCO films can be grown on Y_2O_3/YSZ double buffer layers on Si(100) [24], Y_2O_3 is cubic with a = 10.6 Å and does not provide a c-axis match to YBCO, suggesting that this buffer system may likewise lead to grain boundary nucleation problems. On the other hand, $LaAlO_3$ and $SrTiO_3$ substrates have been successfully used for fabrication of edge-gcolnctly weak links with ion-milled edges [2,4,5,25]. Although these cubic materials do not have lattice constants close to the c-axis of YBCO, thein lattice constants arc very close to one third of the YBCO c-axis so that an effective lattice match is still possible. In addition, cross-sectional transmission electron microscopy (TEM) studies of YBCO films on $LaAlO_3$ and $SrTiO_3$ show no evidence for reaction with YBCO at typical growth temperatures [?6,??]. These results suggest that

$LaAlO_3$ and $SrTiO_3$ buffer layers on SOS should be compatible with edge junction fabrication. Sections 4 and 5 examine YBCO film growth and icdge-geometry weak ink fabrication on $SrTiO_3$-based buffer layer systems on OS.

3. YBCO films and SNS weak links on YSZ buffer layers on SOS substrates

Fabrication of YBCO films and devices on Si or SOS substrates requires a buffer layer to prevent reaction between YBCO and Si. The most commonly used buffer layer has been cubic zirconia, because YSZ buffer layers grown epitaxially on Si enable the growth of high-quality YBCO overlayers. Following the work of Fork and coworkers [7], wc developed a YBCO film growth process over YSZ buffer layers on HF-cleaned SOS substrates. More recently wc have used a modified cleaning process which relies on ZrO_2 reduction of the native SiO_2 layer on the Si surface [12,24,?8]. The r-plane $\{1\ \bar{1}02\}$ SOS substrates are obtained commercially [29], and come with nominally undoped, 0.3 μm thick Si epilayers. With the standard HF-cleaning process, the etched SOS substrates arc mounted with clips on a Haynes metal frame with a hole slightly smaller than the 1/2. inch square substrate, and immediately loaded into the (imposition system. The substrates are radiantly heated to the growth temperature in vacuum, a small amount (≈ 10 Å) of YSZ is deposited, and then 1 mT of oxygen is admitted arid the YSZ deposition is completed. The modified cleaning process also begins with an HF etch, but the substrates arc then mounted on a Haynes metal backing plate with silver paint and baked on a hot plate in air at ≈ 100"C for 20-30 minutes, resulting in reoxidation of the Si surface. The YSZ deposition then proceeds as usual, with the initial YSZ layer deposited in vacuum, which is reported to reduce the native Si oxide layer [1 2,24,28].

The YSZ deposition is followed by growth of a YBCO layer at nominally the same temperature, but with a higher oxygen pressure (120-400 mT). The actual growth temperatures arc not well known with the radiant heating process, but arc estimated to be approximately 800 C. With the silver-paint-mounteci substrates, growth temperatures are 775 - 800°C, as measured by a pyrometer on Si chips mounted adjacent to the device substrate. Typical YSZ buffer layer and YBCO base electrode thicknesses arc 0.2 μm and 0.15 μm, respectively, and the YBCO film

electrical properties are comparable to films grown on $LaAlO_3$ substrates. Following deposition of the YBCO base electrode and the overlying passivation layer, our standard edge junction process was used to fabricate SNS weak links with 150 Å $PrBa_2Cu_3O_{7-x}$ (PBCO) normal metal layers and 1400 Å YBCO counterelectrodes. The total YBCO thicknesses were kept below 3000 Å to minimize potential problems with thermal-stress-induced cracking of the YBCO films.

Figure 2 shows typical current-voltage (I-V) characteristics for a YBCO SNS edge-geometry weak link on a YSZ buffer layer on silicon-on-sapphire with a 150 Å PBCO norm] metal layer at 4.2K. These electrical characteristics clearly suggest the presence of a second weak link in series with the PBCO weak link. The most likely explanation of a series weak link is the formation of a grain boundary in the YBCO counterelectrode. Such a grain boundary could nucleate at the interface between the YBCO base electrode and the YSZ buffer layer. We have used cross-sectional high-resolution transmission electron microscopy (HR TEM) to examine this interface in unpatterned YBCO/YSZ bilayers and found that a thin 30-50 Å reaction layer forms between the YBCO and YSZ. Other workers have also observed this reaction layer and indentified it as $BaZrO_3$, which has a cubic perovskite structure with a lattice constant of 4.2, Å [23,30]. A grain boundary could nucleate at the YBCO-YSZ interface either due to this lattice-mismatched reaction layer; due to the lattice mismatch in the c-axis between the PBCO and YBCO overlayers and the YSZ buffer (a = 5.14 Å); or due to reaction between the PBCO normal metal layer and the YSZ buffer. We have found that the I-V characteristics of SNS weak links fabricated on YSZ buffer layers on $LaAlO_3$ also show double-weak-link behavior, whereas devices produced directly on $LaAlO_3$ do not, confirming that the YSZ buffer is causing the series-weak-link problem, rather than some stress-related or other effect associated with the SOS substrates. Other recent work has aiso shown that YSZ substrates lead to grain boundary nucleation problems in I ITS edge-geometry devices [31]. Although the exact cause of the series weak link is not known at this point, it is clear that there is a problem related to the YSZ buffer layers, and an alternate buffer layer system is needed for weak link fabrication on silicon-on-sapphire substrates.

4. YBCO films on $SrTiO_3$-based multilayer buffers on SOS substrates

4.1 *YBCO/$SrTiO_3$/YSZ/SOS heterostructures*

Because the interface between the YBCO base electrode and the YSZ buffer layer apparently leads to grain boundary formation in the edge junction counterelectrodes, direct contact between the YBCO base electrode and YSZ should be avoided. In principal, the YSZ could be eliminated entirely by using a buffer layer such as $SrTiO_3$ (S"TO). S"1'0 is compatible with edge-geometry weak link fabrication, because it provides an effective c-axis lattice match to YBCO ($3a_{STO} \approx c_{YBCO}$), and does not react with YBCO at normal growth temperatures, as discussed earlier. STO has a relatively high dielectric constant, but this should not have a significant effect for S"1'0 thicknesses much less than a wavelength at the frequencies of interest. However, it has also been found that STO does not grow epitaxially on the Si (1 00) sur face [8], so that direct growth of an S"1'0 buffer layer on SOS is probably not possible and another process is necessary. Because cubic zirconia does grow well on Si(100), an obvious alternate approach is to grow STO over a YSZ buffer layer on SOS as shown in Figure 3. In a test of this method, wc used pulsed- laser deposition to grow YBCO/STO/YSZ heterostructures on SOS substrates. The basic growth process is similar to that described in the proceeding section, except that the intermediate STO buffer layers were generally grown at oxygen pressures of 120-200 ml"' at nominal temperatures approximately 40°C below the YSZ and YBCO growth temperature. Typical layer thicknesses were 1200 - 1500 Å for the YBCO, 1500-2000 Å for the STO, and 400-800 Å for the YSZ.

The structural properties of the YBCO/$SrTiO_3$/YSZ/SOS multi layers were studied using x-ray diffraction and cross-sectional HRTEM, and the superconducting properties of the YBCO were examined by ac susceptibility tests. These studies indicate that the S-l'O does not grow epitaxially on the underlying YSZ buffer layer, resulting in a very poor quality YBCO top layer. An x-ray diffraction $\theta - 2\theta$ scan on the sample displayed only (diffraction peaks from the sapphire substrate and the Si and YSZ epilayers: q'here were no YBCO or S-l"O diffraction peaks. The HRTEM cross-sections confirmed the x-ray analysis: the lattice images and electron diffraction patterns showed crystalline Si and YSZ epilayers, but there was no clear boundary between the STO and YBCO

layers, and no long-range crystallinity in those layers. AC susceptibility measurements of the YBCO film on the same sample showed no superconducting transition to below 10 K. These results are all consistent with very poor quality S1"0 growth on the YSZ buffer layer, which is supported by a previous study of epitaxial insulator multilayer growth [32]. The reason that STO does not grow epitaxially on ZrO_2 (100) surfaces may be qualitatively understood by considering the (100) surface terminations of the two materials. In the [100] direction, cubic ZrO_2 consists of alternating anion and cation planes, while $SrTiO_3$ consists of alternating Sr-O and $Ti-O_2$ (i.e. mixed anion-cation) layers. An epitaxial interface would thus require ions of the same charge to be in close proximity, which is energetically unfavorable.

4.2 YBCO/$SrTiO_3$/YBCO/YSZ/SOS heterostructures

Although S1'0 does not grow epitaxially on YSZ buffer layers, a relatively simple modification of the structure shown in Figure 3 produces a dramatic improvement in the epitaxial quality of the STO and YBCO overlayers. This modification is based upon the observations that YBCO (and analogs, such as PBCO) exhibit high-quality epitaxial growth on YSZ, anti S"1"0 is known to grow epitaxially over YBCO epilayers. Hence the addition of a thin YBCO (or PBCO) "seed layer" over the YSZ buffer on the SOS substrate should serve as a growth template for epitaxy of the S1'0 and YBCO overlayers. The basic idea is illustrated in Figure 4. We have produced heterostructures of this type, anti do, in fact, see a remarkable improvement in the S"1'0 and YBCO film quality relative to structures without the seed layer, as determined by x-ray diffraction, ac susceptibility, and HRTEM measurements.

The film growth process and layer thicknesses for the structure shown in Figure 4 arc the same as the process described in the previous sections, except that a thin (100-250Å) YBCO or PBCO film is grown using our standard laser ablation process just before growth of the S-l'O. X-ray .0- 2θ scans of multilayers produced in this way show all the expected STO and YBCO $(00l)$ diffraction peaks, indicating that the STO and YBCO layers arc c-axis-oriented, unlike structures without the YBCO seed layer. In addition, ac susceptibility measurements reveal a dramatic improvement in the superconducting properties of the YBCO top layer. Figure 5 presents ac susceptibility data for a

YBCO/STO/YBCO/YSZ/SOS heterostructure with a 100 Å YBCO seed layer, which shows a sharp superconducting transition with an onset at 89.6 K and a transition width of 0.6 K. Similar transitions are seen for heterostructures incorporating PBCO seed layers. These results are comparable to our best films on $LaAlO_3$ and should be contrasted to the same measurements made on structures without the YBCO seed layer, which were not superconducting above 10 K. Using a cleavage technique for sample preparation, cross-sectional HRTEM studies were also done on these samples. Figure 6 shows a TEM cross-section of a YBCO/STO/YBCO/YSZ/SOS heterostructure and convergent-beam-electron-diffraction patterns for each layer except the thin YBCO seed layer. The magnified views of the YBCO seed layer and the YBCO top layer show that the YBCO films are epitaxial and c-axis-oriented. The bottom of the YBCO seed layer also shows the expected $BaZrO_3$ reaction layer at the YBCO-YSZ interface. Although difficult to see on the scale of the figure, clean lattice fringes are present for the Si, YSZ, and S"1'0 layers, and the electron diffraction patterns confirm that all layers are epitaxial.

'l'he x-ray, ac susceptibility, and HRTEM studies demonstrate that incorporation of a YBCO or PBCO seed layer leads to a dramatic improvement in the epitaxial quality of the STO and YBCO overlayers. More quantitative studies of the epitaxial quality of these heterostructures are in progress, while SNS device fabrication and results on the electrical transport properties of the top YBCO layer are discussed in the following section.

5. SNS weak links on STO/YBCO/YSZ buffer layers on SOS

Using the STO/YBCO/YSZ multi layer buffer system, wc have fabricated high-quality, epitaxial, edge-geometry SNS devices on SOS substrates, which show no evidence for series grain-boundary weak links. The structure shown in Figure 4 serves as the starting point for device fabrication, with the top YBCO film becoming the base electrode of the completed SNS edge junction. Weak links have been produced with both PBCO and Co-doped-YBCO normal metal layers. We utilized our standard edge junction process for device fabrication, with base electrode

YBCO thicknesses of 1200 - 1500 Å, oxide normal metal thicknesses of 65 - 150 Å, and counterelectrode thicknesses of 1100 -1600 Å.

The current-voltage (I-V) characteristics for-atypical YBCO/PBCO/YBCO edge-geometry weak link on STO/YBCO/YSZ buffer layers on a silicon-on-sapphire substrate are shown in Figure 7. The PBCO thickness is 65 Å and the temperature is 65 K. The electrical characteristics are qualitatively consistent with the resistively-shttnted junction (RSJ) model, although there is a significant amount of excess current. The weak-link critical current density, J_c, is 3.4 x 10'1 A/cm^2, the I_cR_n product is 145μV, and the R_nA product is 4.3 x 10-9 Ω-cm^2. These results are consistent with results obtained for PBCO devices on $LaAlO_3$ substrates [5]. The PBCO weak links on SOS also exhibited ac Josephson steps, which showed the expected voltage spacing and modulated with varying microwave power. The most important point to note is that the I-V data for this device shows no indication of the series weak links that were seen in edge junctions fabricated directly on YSZ buffer layers (see Figure 2), even for currents an order of magnitude larger than shown in Figure 7. This suggests that the multilayer STO/YBCO/YSZ buffer system is, in fact, preventing grain-boundary nucleation at the base-clcctl'oc] c-Y13C()/illsLllator interface, presumably because $SrTiO_3$ provides a c-axis lattice match to PBCO and YBCO, and does not react at the growth temperature.

Figure 8(a) shows the I-V characteristics at 70 K for an edge-geometry SNS weak link on a STO/YBCO/YSZ multilayer buffer on a silicon-on-sapphire substrate using a 150 Å $YBa_2Cu_{2.8}Co_{0.2}O_{7-x}$ (YBCCO) normal metal layer. Co-doped YBCO with a Co-doping level of 0.2 has a transition temperature of approximately 40- 50 K, and has previously been used to fabricate high quality SNS devices on $LaAlO_3$ substrates in our own laboratory and elsewhere [33]. As can be seen in Figure 8(a), the electrical characteristics of the YBCCO weak links on SOS are also qualitatively consistent with the RSJ model, although there is some excess current. The electrical parameters of this device at **70** K are J_c = 1.2 x 10^5 A/cm^2, I_cR_n = 140 μV, and R_nA = 1.2 x 10^{-9} Ω-cm^2, which are consistent with our previous YBCCO device results on $LaAlO_3$. The microwave response of the YBCCO weak link under 14.4 GHz irradiation is presented in Figure 8(b). As with the PBCO devices, the ac Josephson steps occur at the expected voltage spacings and periodically

modulate to zero as the applied microwave power is varied. At 77 K, the electrical parameters of this device are $J_c \approx 1.9 \times 10^4$ A/cm^2, $I_cR_n \approx 30$ μV, and $R_nA \approx 1.6 \times 10^{-9}$ Ω-cm^2, as shown in Figure 9(a). Figure 9(b) shows a large-range curlellt-voltage sweep for the same YBCCO weak link. Three is no evidence for a series grain boundary weak link, but a gradual transition to higher resistance is apparent at drive currents above approximately 3.5 mA. This transition is believed to correspond to the critical current density of the YBCO counterelectrode, giving an electrode J_c of= 1.3×10^6 A/cm^2 at 77 K. Separate measurements of patterned bridges in the base and counter-electrode YBCO layers on this chip and several other chips indicate current densities in the range of 5×10^5 to 2×10^6 A/cm^2 for both YBCO layers at 77 K. These J_c values are close to the current densities seen for high-quality single layer YBCO films on $LaAlO_3$ ($\approx 3 \times 10^6$ A/cm^2), and further optimization of the buffer layer and YBCO growth processes is expected to lead to even higher electrode current densities on SOS.

The PBCO and YBCCO device results demonstrate that the addition of the YBCO seed layer and the STO buffer layer above the YSZ buffer enables the fabrication of high-quality edge-geometry SNS weak links on silicon-on-sapphire substrates. SNS weak links fabricated on this multilayer buffer system on SOS are comparable in quality to our best devices on $LaAlO_3$, and show no evidence for series grain boundary weak links. High J_c values are obtained for both the base and counterelectrode YBCO layers. This development provides the technology necessary for ultra-high-frequency HTS superconducting device applications, as well as enabling the integration of superconductor and semiconductor circuitry. From a circuit perspective, this approach also has the advantage that a superconducting ground plane can be naturally incorporated into the device structure simply by using a thicker YBCO seed layer.

A potential drawback of this approach is the relative complexity of the STO/YBCO/YSZ multi-layer buffer system, but the process has proven to be reliable and reproducible. Another possible problem is a thickness limit on the YBCO overlayers, due to stress-induced cracking caused by the thermal expansion mismatch between YBCO and sapphire. Reported YBCO thickness limits on SOS range from 2000 to 4000 Å [13,1 4]. In the present work, wc have been careful to limit the total

YBCO thickness of the base plus the counterelectrode to around 3000 Å, and have seen no obvious problems with film cracking. However, thermal stress problems could become more serious for multilayer circuit applications incorporating ground planes and epitaxial insulators. "l'here have also been reports of long term degradation of YBCO thin films on silicon due to thermal stress effects [11,1 2]. Aging effects should be less serious with SOS substrates, because the thermal expansion coefficients of YBCO and sapphire arc more closely matched, but it will be important to examine long-term stability of devices on SOS. It should also be noted that the use of multiple buffer layers may help reduce aging effects and stress cracking in the films, because stress-relieving misfit dislocations can be introduced at the heteroepitaxial interfaces [12].

6. Summary

SOS substrates have the advantages of a moderate dielectric constant, a reasonable thermal-expansion match to YBCO, and offer the possibility of integration with Si circuitry. Devices fabricated directly on single YSZ buffer layers on SOS exhibit series weak links that appear to be associated with grain boundary nucleation at the base-YBCO/YSZ interface. To eliminate this problem, wc developed a multilayer buffer system which consists of an epitaxial STO/"seed-layer"/YSZ heterostructure grown on an SOS substrate. The novel feature of this approach is the incorporation of the thin YBCO or PBCO seed layer which serves as a template for growth of a high-quality STO overlayer. YBCO/STO/seed-lay er/YSZ/SOS heterostructures show a dramatic improvement in S1'0 and YBCO film quality relative to structures which do not incorporate the YBCO seed layer. In addition, SNS junctions fabricated on STO/YBCO/YSZ buffers with PBCO or Co-doped YBCO normal-metal layers exhibit greatly improved electrical characteristics, with RSJ-like I-V characteristics, modulating ac Josephson steps, and no evidence for series grain boundary weak links. This is the first demonstration of high-quality, epitaxial, ecl~c-geometry SNS weak links on SOS substrates, and provides a key technology for ultra-high-frequency IITS superconducting device applications, as well as for integration of superconductor and semiconductor circuitry.

7. Acknowledgements

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Figure Captions

Figure 1. (a) Schematic cross-sectional diagram of an edge-geometry YBCO/normal-metal/YBCO SNS weak link with c-axis-oriented YBCO thin films. The double arrow illustrates current flow through the active area of the device. (b) Cross-section of an edge junction showing a grain boundary in the counterelectrode. Such a grain boundary can nucleate at the base YBCO - buffer layer interface if a reaction layer exists or there is a c-axis mismatch between the buffer layer and the normal metal and counterelectrode.

Figure 2. Current-voltage characteristics for a YBCO edge-geometry weak link on a YSZ buffer layer on an SOS substrate with a 150 Å PBCO normal metal layer at 4.2 K. The counterelectrode is 3 μm wide and 0.14 μm thick, and the base electrode is 0.15 μm thick. The I-V curve suggests the existence of a series grain-boundary weak ink, The vertical scale is 100 μA/div. and the horizontal scale is 200 μV/div.

Figure 3. Schematic cross-section of a YBCO/$SrTiO_3$/YSZ/SOS heterostructure. Studies indicate that the STO layer does not grow epitaxially over YSZ, and that the YBCO is not superconducting.

Figure 4. Schematic cross-section of a YBCO/$SrTiO_3$/YB CO/YSZ/SOS heterostructure. The addition of a thin YBCO (or PBCO) seed layer results in a dramatic improvement in the epitaxial quality of the STO and YBCO overlayers.

Figure 5. In-phase (circles) and out-of-phase (triangles) ac susceptibility data for a YBCO/STO/YBCO/YSZ/SOS heterostructure with a 100 Å YBCO seed layer and a 1200 Å YBCO overlayer. The transition onset is 89.6 K with a transition width of 0.6 K. Similar structures, but without a YBCO seed layer, show no superconducting transition to below 10 K.

Figure 6. Cross-sectional TEM micrograph of YBCO/STO/YBCO/YSZ/SOS heterostructure from a portion of the same chip as measured in Fig. 5, with convergent-beam electron diffraction patterns from each layer. The lattice fringes and diffraction patterns indicate that all layers are epitaxial, in contrast to heterostructures which do not include the thin YBCO seed layer.

Figure 7. I-V characteristics for a YBCO edp,c-geometry weak link on a STO/YBCO/YSZ multilayer buffer on an SOS substrate with a 65 Å PBCO normal metal layer at 65 K. The counter-electrode is 1.8 *pm* wide and 0.11 μm thick, and the base electrode is 0.12 pm thick. The electrical characteristics show no evidence for a series grain-boundary weak link. The vertical scale is 100 μA/div. and the horizontal scale is 50 μV/div.

Figure 8. I-V characteristics for a YBCO edge-geometry weak link on a STO/YBCO/YSZ multilayer buffer on SOS with a 150 Å $YBa_2Cu_{2.8}Co_{0.2}O_{7-x}$ normal metal layer at 70 K. The counterelectrode is 1.8 μm wide and O. 16 μm thick, and the base electrode is 0.15 μm thick. (a) No applied microwave power. The electrical characteristics show no evidence for a series grain-boundary weak link. (b) ac Josephson steps under 14.4 GHz irradiation. The critical current has been suppressed to zero at this microwave power. The vertical scale is 500 μA/div. and the horizontal scale is 50 μV/div.

Figure 9. I-V characteristics for the same device as in Figure 8, except at 77 K with no applied microwave power. (a) Low voltage sweep with vertical scale "of 200 μA/div. and horizontal scale of 50 μV/div. (b) L.argc-range sweep showing counterelectrode transition, but no evidence for series grain boundary weak link. The vertical scale is 2 mA/div. and the horizontal scale is 500 μV/div.

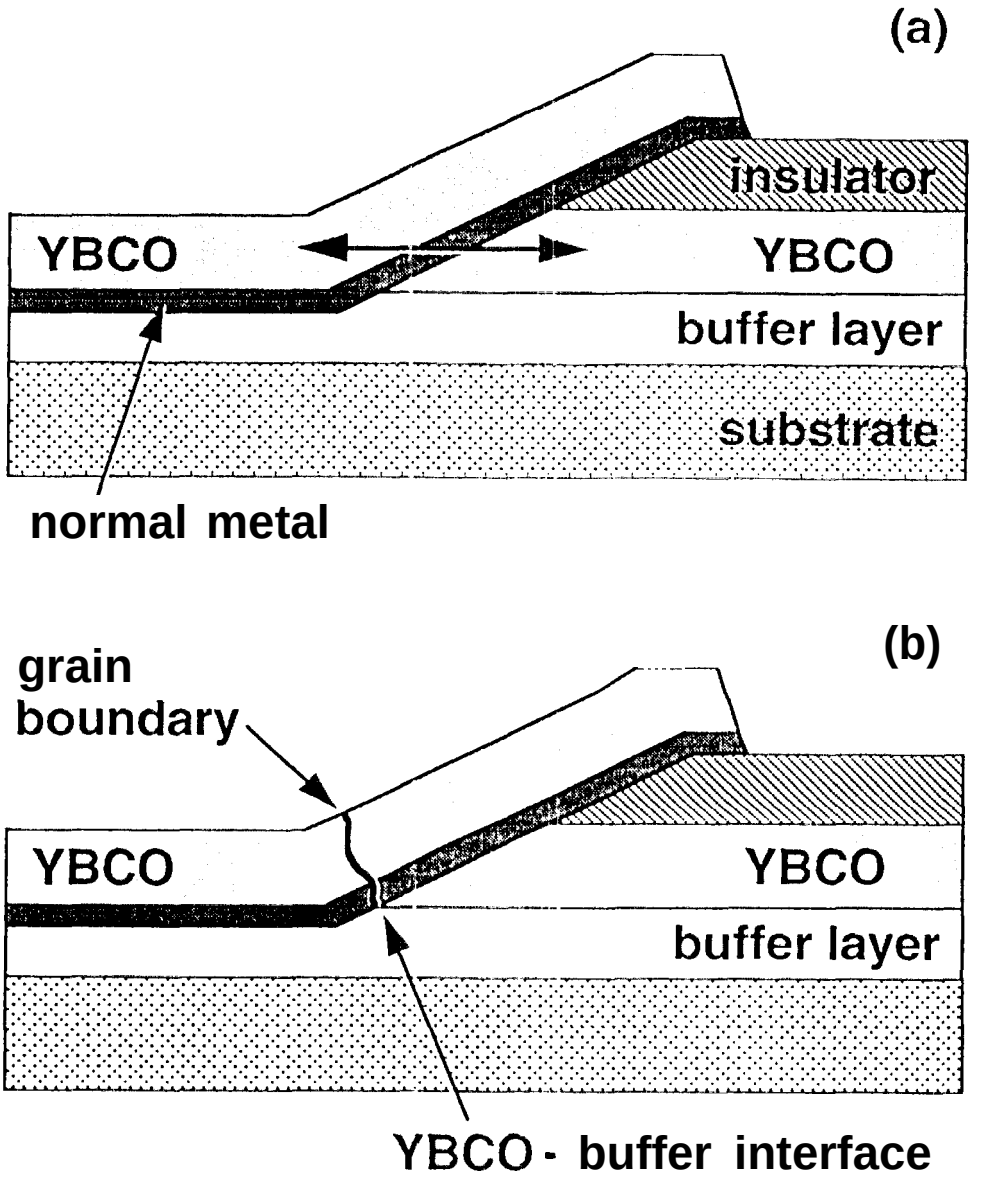
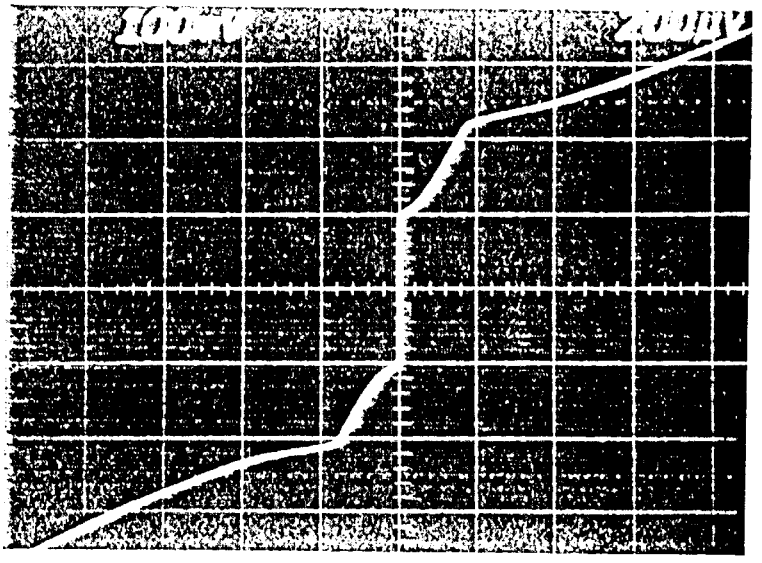

(a)
insulator
YBCO
YBCO
buffer layer
substrate
normal metal
(b)
grain
boundary
YBCO
YBCO
buffer layer
YBCO - buffer interface

Figure 1



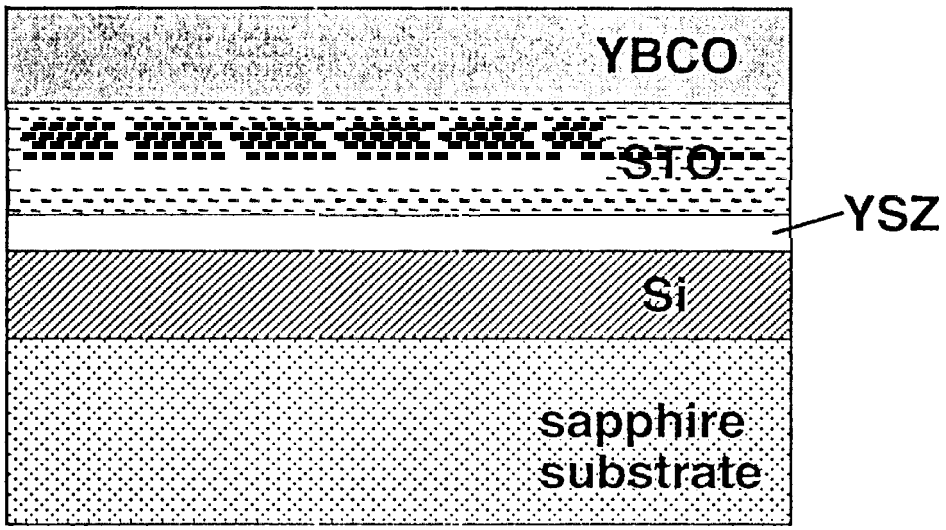


Figure 3

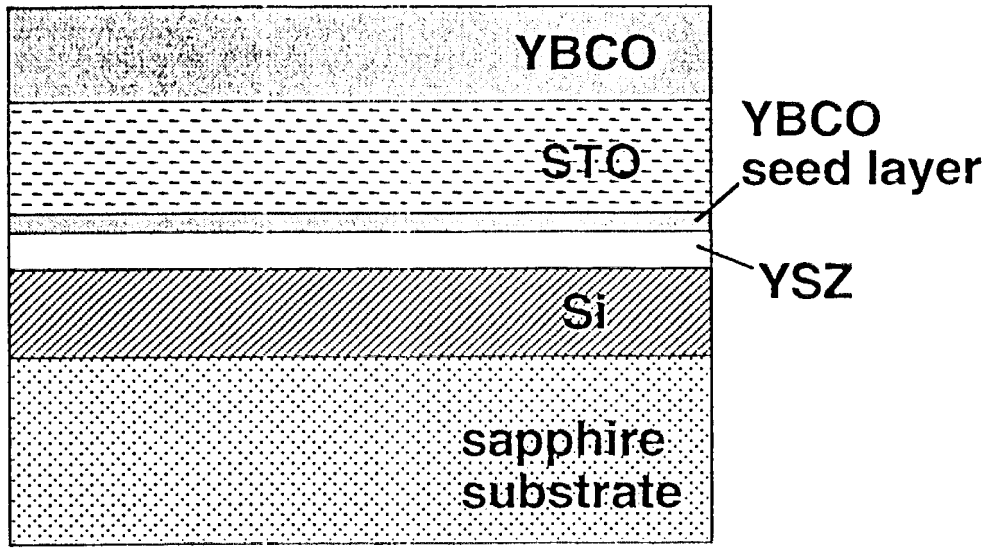


Figure 4

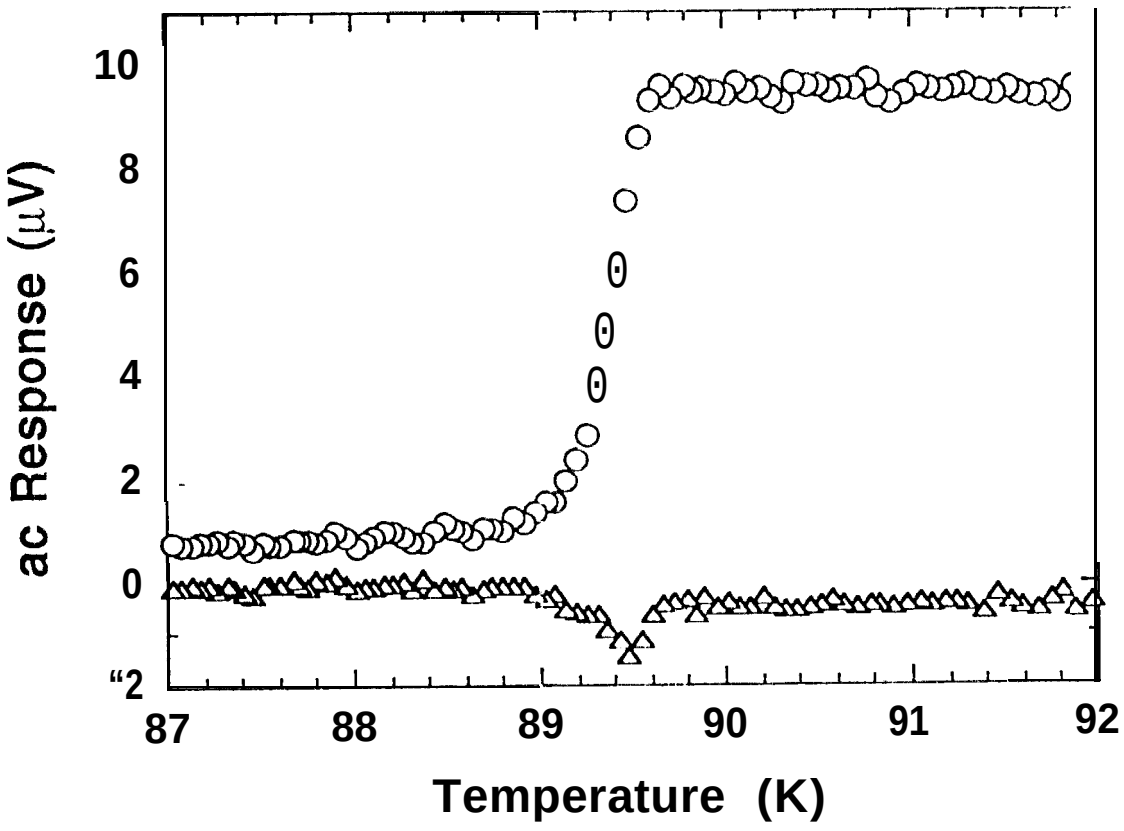


Figure 5

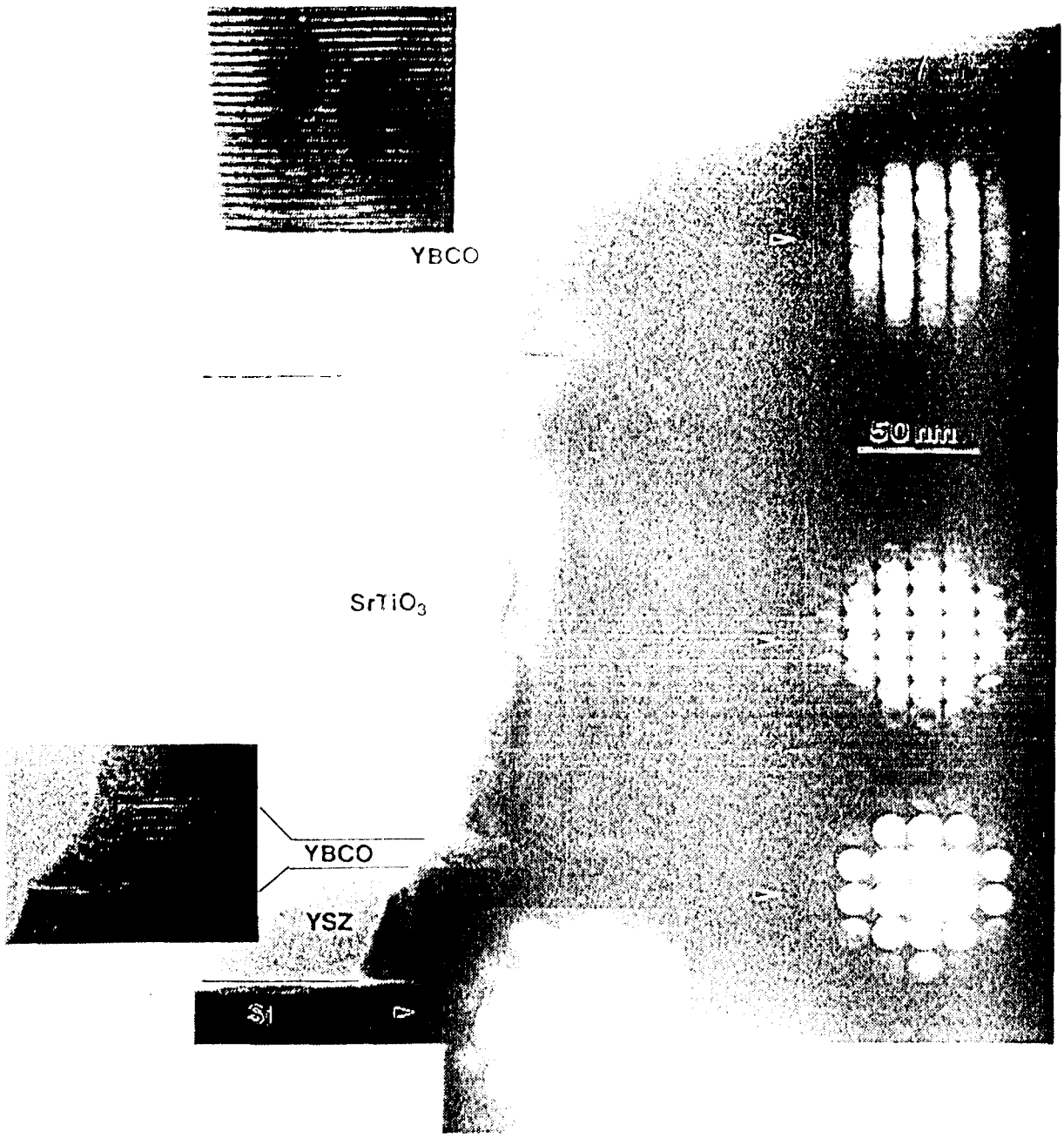


Figure 6

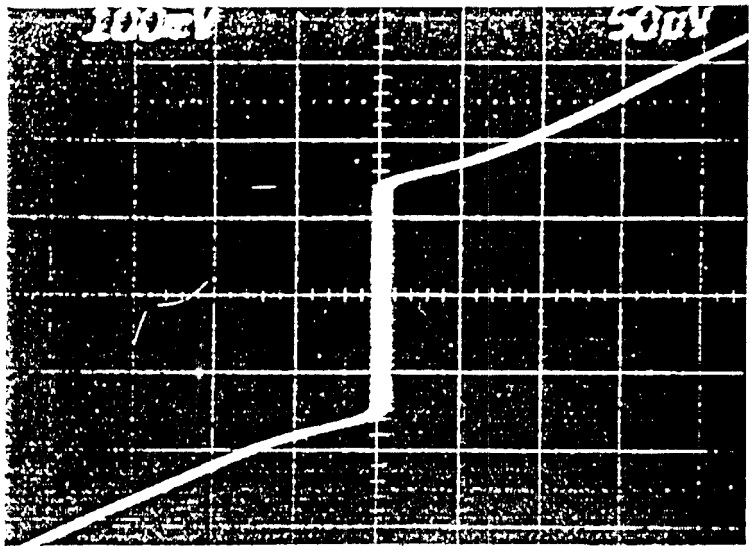
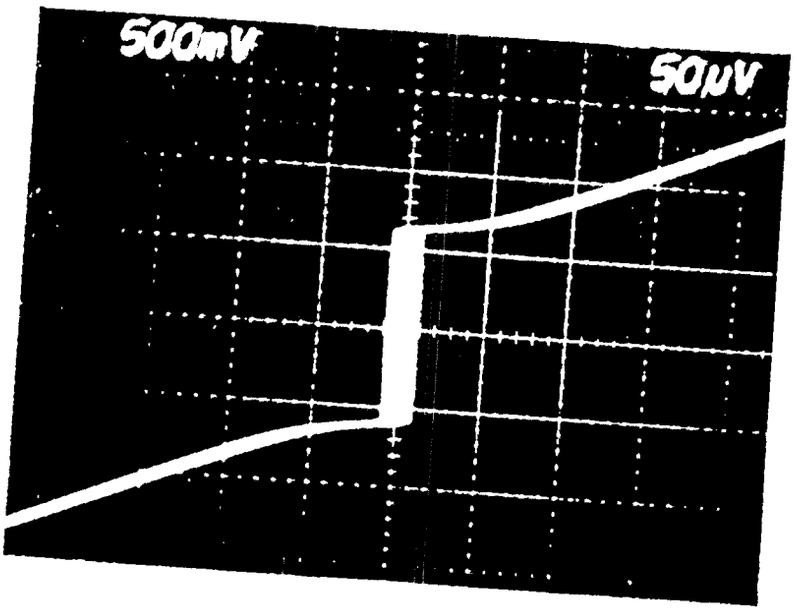


Figure 7

(a)



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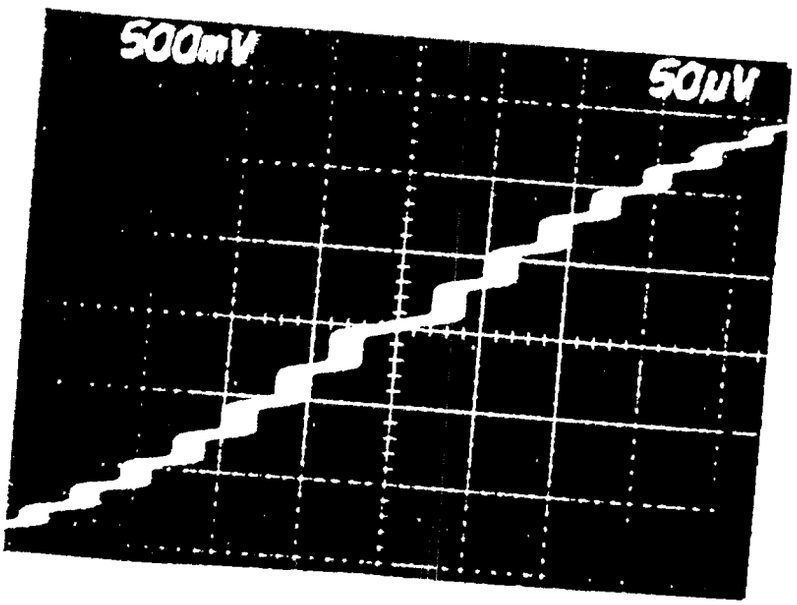
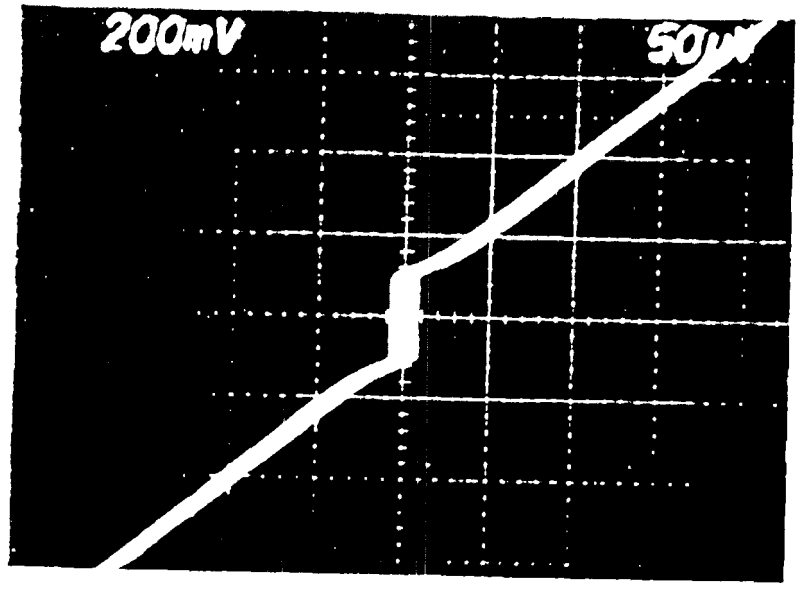
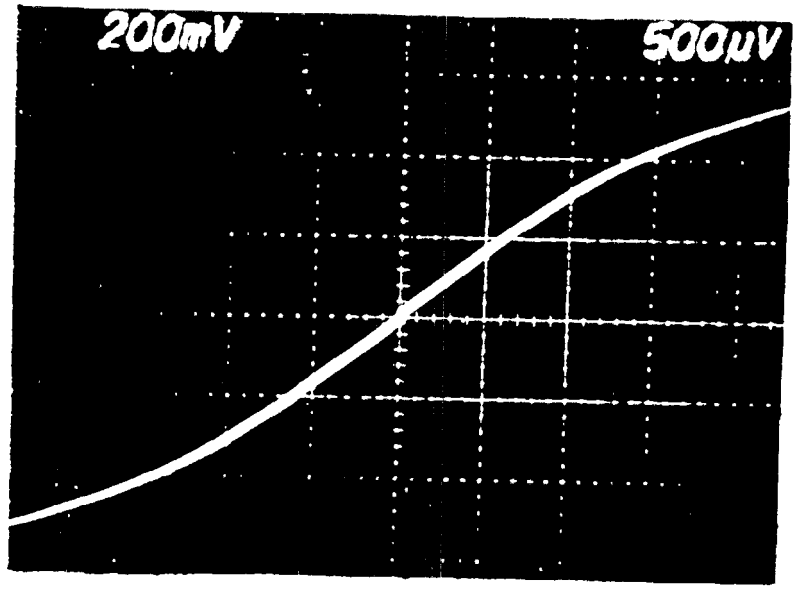


(a)



(b)